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Open Defect Fault Analysis in Single Cell SRAM Using R, and C Parasitic Extraction Method

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***Abstract*—As the technology scaling is increasing, the device density is more prone to parasitic effects that lead to some form of undetectable faults. However, the existing test methods are not adequate to identify such undetectable faults. In this paper we propose a new fault model taking parasitic effects into consideration, to detect the faults along with fault location. The proposed method in this paper is considered node-to -node open defects at the circuit level using 120nm technology. Test results observed with few existing faults like Transition Faults (TF), Incorrect Read Faults (IRF) and No Access Faults (NAF). In addition to these, few more faults in the name of undetectable faults (UDFs) also observed. These faults can easily be identified using proposed parasitic extraction method, in which defect-imposed node gets affected with variation in its parasitic R& C values. Total seven UDFs were observed, and few are mentioned here such as UDF_1 is at the locations of transistor M_1 drain to node Q with observed R value of 3.7 kΩ and C value of 4.7fF. Similarly, UDF2 is observed at nodes M2 drain and Q with corresponding R value of 4.14kΩ and C value of 5.1fF**

Keywords—Parasitic Extraction Method, Deep submicron technology, march algorithm, layout fault model, Open Faults

I. INTRODUCTION

Day to day decrease in nano meter technology allowing the integration dense to grow tremendously leads to an unwanted interconnections or undesired disjunctions, and this may cause several defects in the layout which in turn causes faulty effect in the memory circuits. SRAM memories are more predominant rather than core semiconductor within the total embedded structure. Due to advancement in the technologies, the continuous reduction in the memory cell area causes the occurrence of these defects and thus results in surplus noise and malfunctioned behavior. Earlier inventions reveal the method of fault detection in the form of layout defect transformation into circuit level fault model [1] and use of algorithm to detect the faults. In this process fault models are confined to the level of detectable faults and the scope for undetectable faults is minimized. Undetectable faults are the faults whose behavior resembles the fault free cell behavior. Most of the literature considered the electrical level fault models [2] which are easy in analyzing the faulty behavior. But the test time complexity is a major drawback that last in algorithm-based testing methods. Initially numerous defects models were followed on simple stuck at and transition fault models, but later on the work was enhanced to dynamic faults, linked faults, and realistic faults models [3, 4]. These fault models followed a simple electrical structure like bridge or open between two nodes within the cell, or between the two cells. Single cell fault models were analyzed with the help of primitive based March test algorithms. Delve of March primitive operations in the form of algorithms were used in order to improvise the fault coverage [5]. Despite to the fault coverage, increase in March primitives increases the test complexity in terms of test time and hardware implementation. Further fault detection was carried out on linked faults [6] which are more complex as they involved with more than one cell. Apart from these traditional classical fault models, few more faults were found under non-classical such as address decoder faults [7]. Every part of cell was considered for modeling the faults in order have the benefit of complete fault detection picture pertain to single cell. When the Based on the number of operations chosen in detecting the fault, static and dynamic faults were characterized and exploited the extensive use of March algorithms [8]. But both dynamic and linked faults are complex to identify, and also test time grows up once the memory size is going up.

Defect based test analysis is more predominantly observed using fault location resistance and capacitance variations [9]. The fault locations were selectively chosen in the layouts and applied short or open defects for observing the faulty behaviors in the corresponding electrical circuit models [10, 11, 12, 13, 14, 15, 16, 17, 18,19 & 20]. Resistive-opens/shorts are generally coming under the category of timing-dependent fault models through which one can estimate the delay response of the circuit. In order to identify the fault due to resistive open/short, a two-pattern sequence is usually needed to sensitize the fault, but to be performed at-speed in contrast to stuck open faults. Moreover, the resistive-open defects have predominantly significant to be considered due to increased number of interconnection layers in the recent technologies. March algorithms used to detect faults, but these algorithms need a specific sequence. To detect delay faults, we require speed test. In particular in [20] gate oxide shorts report resistive short defects and metal disjunctions may cause resistive open defects. These are the most common defects that escape the test seen in deep sub-micron technologies. Resistive-open defects are the main focus in this study as there is a huge gap observed in this research area. Resistive open defects have been injected in the core-cell of SRAM electrical circuit's models and observed the defect behavior in the corresponding layout. Section II is focused on existing work on resistive open defect models, section III will discuss about proposed fault model for resistive open defects. Section IV continues with results, and section V will discuss the conclusions.

II. OPEN DEFECT MODELS

Open resistive faults are produced during the manufacturing time of 6T SRAM. The behavior of the memory cell may modify by these open faults. The types of open faults are, stuck - open faults and resistive open faults,

stuck-open faults are special case, where the resistance value is very high, for the resistive open faults it is defect of resistance between the nodes. [10] used three test conditions such as supply voltage, speed and temperature for detecting stuck-open and resistive open faults. To detect resistive open defects such as Read Destructive Fault (RDF) static and dynamic, Deceptive Read Destructive Fault (DRDF), Incorrect Read Fault (IRF) and Transition Fault (TF) [16] proposed a single march test. Analysis of fault model using March tests able to give the information only on detection of faults. But March algorithms fail to give the information about bit line capacitance influence while reading or writing the data, propagation delay analysis and dynamic power analysis [19-20] suggested a method with the help of layout model by considering these constraints. Due to scale down technology, changes in parasitic effects may cause faults in memory [21] proposed a parasitic extraction method to detect the fault and location of the fault. In this method to detect fault induced SRAM, extracted parasitic R and C values of fault free SRAM are used to compare the extracted R and C values of faulty model.

III. PROPOSED METHOD OF PARASITIC EXTRACTION

Typical CMOS 6T SRAM consist six transistors M_1 to M_6. Transistors M_1 and M_2 form one inverter, where as M_3 and M_4 forms another inverter, these are cross coupled inverters. M_5, M_6 are pass transistors, BL, BLB are bit lines, used for read and write operations. Q, Q_B are internal nodes used to analyze the cell data. Fig.1 shows the proposed open defect model. We used node to node analysis. For simplicity OF is used for Open Fault.

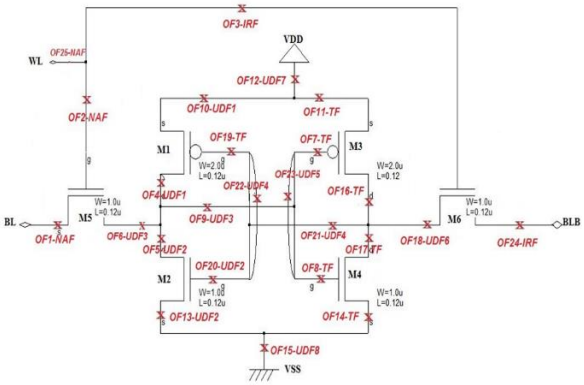

Fig. 1. Proposed fault model for open defects

TABLE I. FAULT DICTIONARY FOR SINGLE CELL 6T SRAM

S. No	*Open Defect*	*Defect Model*	*Fault Models*
1	BL-M_{5S}	OF_1	NAF
2	WL- M_{5G}	OF_2	NAF
3	WL- M_{6G}	OF_3	IRF
4	Q-M_{1D}	OF_4	UDF_1
5	Q-M_{2D}	OF_5	UDF_2
6	Q-$M_{1D}M_{2D}$	OF_6	UDF_3
7	Q-M_{3G}	OF_7	TF
8	Q- M_{4G}	OF_8	TF
9	Q-$M_{3G}M_{4G}$	OF_9	UDF_3
10	V_{DD}-M_{1S}	OF_{10}	UDF_1
11	V_{DD}-M_{3S}	OF_{11}	TF
12	V_{DD}-$M_{1S}M_{3S}$	OF_{12}	UDF_6
13	V_{SS}-M_{2S}	OF_{13}	UDF_2
14	V_{SS}-M_{4S}	OF_{14}	TF
15	V_{SS}-$M_{2S}M_{4S}$	OF_{15}	UDF_7
16	Q_B - M_{3D}	OF_{16}	TF
17	Q_B - M_{4D}	OF_{17}	TF
18	Q_B_$M_{3D}M_{4D}$	OF_{18}	UDF_5
19	Q_B_M_{1G}	OF_{19}	TF
20	Q_B_M_{2G}	OF_{20}	UDF_2
21	Q_B_$M_{1G}M_{2G}$	OF_{21}	UDF_4
22	M_{1G}_M_{2G}	OF_{22}	UDF_4
23	M_{3G}_M_{4G}	OF_{23}	UDF_3
24	BLB - M_{6S}	OF_{24}	IRF
25	WL-$M_{5G}M_{6G}$	OF_{25}	NAF

Functional Fault Model (FFM) is the difference between the observed and expected one. By using Fault Primitives (FPs). Faults will be identified using existing FPs. Undetectable faults cannot be identified using existing FPs. Using our Parasitic Extraction method, we can identify both existing and undefined faults

The existing faults identified are Incorrect Read Fault (IRF) if read operation of the cell gives the incorrect value by keeping the correct value in the cell is called IRF, Transition Fault (TF), if we will not able to write 0, in the cell where 1 is already stored vice versa is called transition fault. No Access Fault (NAF), if we are not able to perform any read or write operation on the cell is called NAF as shown fig.2.

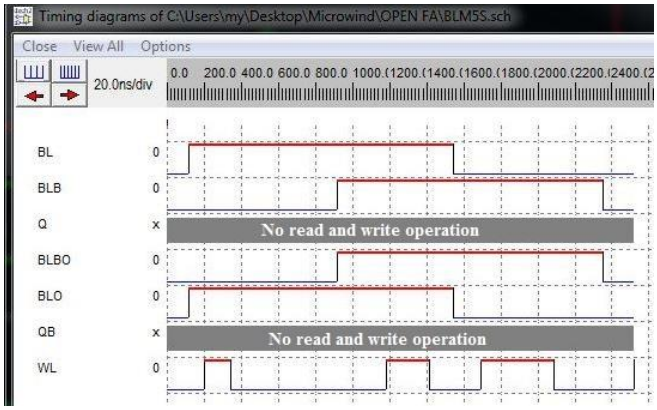

Fig.2. Simulation results for No Access Faults

Using R and C Parasitic Extraction method, undetected fault can be found which are named as Undefined Faults (UDF). As there are seven undetected faults are identified and are named as Undefined Faults. We found undefined fault 1 (UDF_1) at

the nodes of Q, drain of transistor M1and same defect identified at nodes V_{DD}, source of the transistor M_1.

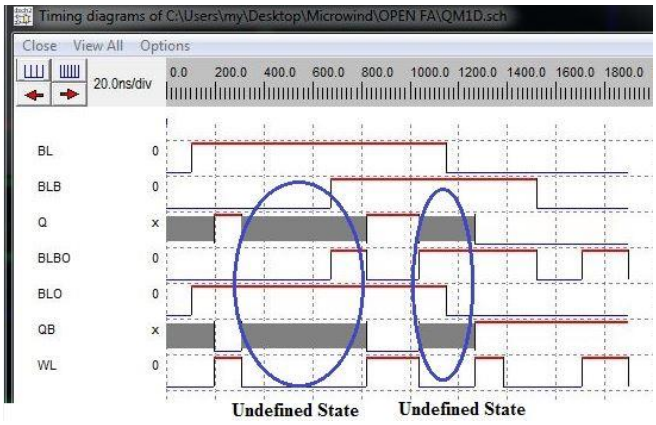

Fig.3. Simulation results for Undefined Fault 1

As shown in the fig.3, while performing write 1 operation and read 1 operation the is holding the correct value until write line is high, when write line value is low the cell is going to undefined state. While performing write zero and read zero operations the behavior of the cell is normal. Undefined Fault 2 (UDF_2) detected at nodes Q, drain of the transistor M_2, and node Q_B, gate of transistor M_2 and at nodes V_{SS} and source of M_2.In UDF_2 it is observed that for write 1, read1 and write 0 there is no error in the cell, after write 0 operation whenever write line goes low, the cell goes to undefined state. Undefined Fault 3 (UDF_3) found at nodes Q to, drains of transistor M_1 and M_2 and at nodes Q and gates of transistor M_3 and M_4 and same defect detected at gates of transistors M_3 and M_4, as shown in the fig.4, in UDF_3, it is observed that the node Q_B always in undefined state, where as node Q goes to undefined state whenever write line is low

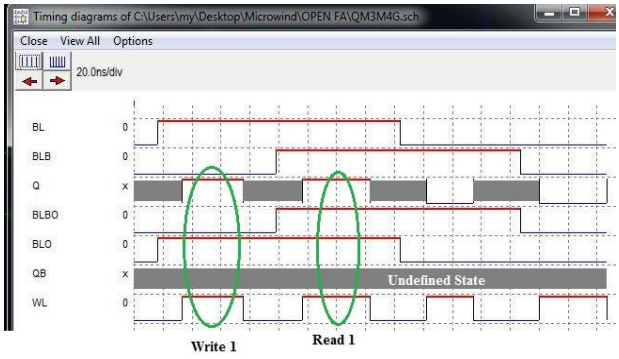

Fig.4. Simulation results for Undefined Fault 3

As shown in the fig.5, in Undefined Fault 4 (UDF_4) the cell goes to the undefined state whenever write line value is low for both write and read operations of zero and one, that is the cell is holding the values of read and write operation only high value of write line, UDF_4 found at node Q_B and gate of transistors M_1 and M_2, same defect we found at gate of transistor M_1 and gate of transistor M_2.where as in Undefined Fault 5 (UDF_5),found at node Q_B and drains of the transistors M_3 and M_4. In this fault it is observed that at node Q_B we cannot perform any read and write operation, such as node Q_B always in undefined state

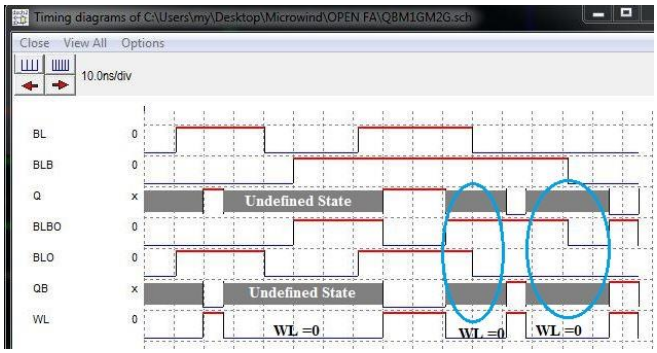

Fig.5. Simulation results for Undefined Fault 4

Undefined Fault 6 (UDF_6) found at node V_{DD} and source of Transistors M_1 and M_3. In UDF_6, for read1 and write 1 operation the cell is holding the values whenever write line is 1 otherwise it goes to the undefined state. Undefined Fault 7 (UDF_7) found at node V_{SS} and source of transistors M_2 and M_4. In UDF_7 the no Q goes to Undefined State, whenever write logic is zero, and at node Q_B, we cannot perform any read and write operations except write 0 operation

IV. Results

In this parasitic extraction method we have used Microwind tool(DSCh2) and a circuit simulator. Options of layout simulator selected as supply voltage is 1.2V, default gate dealy 0.030ns, default wire delay 0.070ns and time unit is 10ps. In this experiment we have consider 120nm technology to design CMOS transistors. In this the length of the pMOS and nMOS transistors are 120nm whereas the width of the pMOS and nMOS transistors consider as 200nm and 100nm respectively as shown in the fig.1. in this experiment we have carried totally 25 open defect fault models. For each fault model we have extracted node resistance and capacitance values, and compared with resistance and capacitance values of fault free SRAM. Table 2. shows the extracted parasitic R and C values for both fault free and fault models at nodes Q, Q_B, WL, BL, BLB, V_{DD}, V_{SS}.

Detection of faults using parasitic extraction method is achieved by comparing parasitic Rand C values of fault model, with parasitic R and C values of fault model. For example, as shown in the fig.6 and fig.7, open defect between node Q and drain of transistor M_1 induced UDF_1. The parasitic C and R values at Q for fault free SRAM is 4.66fF and 7.185kohms respectively, when fault induced between node Q and drain of transistor M_1, the parasitic C and R values changes to 3.7fF and 4.728kohms respectively. whereas at other nodes (Q_B, WL, BL, BLB, V_{DD}, V_{SS}), no change in the parasitic R and C values.

Fig.6 .Fault Detection Based on Parasitic capacitance variation at node Q

Fig.7. Fault Detection Based on Parasitic Resistance variation at node Q

In this way parasitic C and R values will vary at least one node of SRAM when fault induced in the layout. It is observed that by considering input and output nodes parasitic values R and C values equivalent, these faults are called equivalent faults. From the above results we can say that parasitic extraction method gives the 100% fault coverage.

TABLE II. COMPLETE FAULT MODEL DICTIONARY FOR SINGLE 6T SRAM CELL: R, C VALUES

S.No	Open Defect	Defect Model	Fault Models	Node QB Fault Free C = 4.478F, R=6.728 KΩ		Node Q Fault Free C = 4.66fF, R=7.185 KΩ		Node WL Fault Free C = 1.99fF, R= 0.369KΩ		Node BL Fault Free C = 0.93fF, R= 1.157KΩ		Node BLB Fault Free C = 1.03fF, R= 2.095KΩ		Node VDD Fault Free C = 8.25fF, R= 7.064KΩ		Node VSS Fault Free C = 2.04fF, R= 3.605KΩ	
				C in fF	R in KΩ	C in fF	R in KΩ	C in fF	R in KΩ	C in fF	R in KΩ	C in fF	R in KΩ	C in fF	R in KΩ	C in fF	R in K
1	BL-MSS	OF1	NAF	4.47	6.728	4.67	7.185	1.99	0.369	NA	NA	1.01	2.095	8.25	7.064	2.04	3.60
2	WL- M5G	OF2	NAF	4.47	6.728	4.67	7.185	1.23	0.187	0.91	1.157	1.03	2.095	8.25	7.064	2.04	3.60
3	WL- M6G	OF3	IRF	4.47	6.728	4.66	7.185	1.15	0.186	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
4	Q-M1D	OF4	UDF1	4.48	6.728	3.7	4.728	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
5	Q-M2D	OF5	UDF2	4.47	6.728	4.14	5092	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
6	Q-M1DM2D	OF6	UDF3	4.5	6.728	0.93	2094	1.94	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
7	Q-M3G	OF7	TF	4.48	6.728	3.14	6.83	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
8	Q- M4G	OF8	TF	4.47	6.728	3.9	7001	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
9	Q-M3GM4G	OF9	UDF3	4.48	6.728	2.38	6646	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
10	VDD-M1S	OF10	UDF1	4.47	6.612	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	7.67	4.624	2.04	3.60
11	VDD-M3S	OF11	TF	4.47	6.728	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	7.64	4.399	2.02	3.60
12	VDD-M1SM3S	OF12	UDF6	4.47	6.612	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	7.06	1.958	2.01	3.60
13	VSS-M2S	OF13	UDF2	4.47	6.728	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	1.72	246
14	VSS-M4S	OF14	TF	4.47	6.728	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	1.72	246
15	VSS-M2SM4S	OF15	UDF7	4.47	6.728	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	1.39	131
16	QB - M3D	OF16	TF	3.51	4.045	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
17	QB - M4D	OF17	TF	3.97	4.637	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
18	QB_M3DM4D	OF18	UDF5	1	1.158	4.52	7.185	1.94	0.369	0.91	1.157	1	2.095	8.25	7.064	2.04	3.60
19	QB_M1G	OF19	TF	3.2	6.172	4.49	7.185	1.99	0.369	0.93	1.157	NA	NA	8.25	7.064	2.04	3.60
20	QB_M2G	OF20	UDF2	3.73	6.49	4.66	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
21	QB_M1GM2G	OF21	UDF4	2.24	5.933	4.5	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
22	M1G_M2G	OF22	UDF4	2.44	5.933	4.5	7.185	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
23	M3G_M4G	OF23	UDF3	4.48	6.728	2.38	6.646	1.99	0.369	0.93	1.157	1.03	2.095	8.25	7.064	2.04	3.60
24	BLB - M6S	OF24	IRF	4.47	6.728	4.66	7.185	1.99	0.369	0.93	1.157	NA	NA	8.25	7.064	2.04	3.60
25	WL-M5GM6G	OF25	NAF	4.47	6.728	4.67	7.185	NA	NA	0.91	1.157	1.01	2.095	8.25	7.064	2.04	3.60

V. CONCLUSION

In this paper we proposed a novel parasitic extraction method. A layout of fault injected model extracted and compared with fault free layout model. In this paper we consider the node-to-node open defects that gives the complete fault model dictionary. Using this complete fault dictionary, we can find equivalent faults. For equivalent faults the parasitic C and R Values are equal. Using proposed parasitic extraction method, we detected defined faults such as Transition Faults, Incorrect Read Faults, No Access Faults, and also, we found total seven undefined faults denoted as UDF_1, UDF_2, UDF_3, UDF_4, UDF_5, UDF_6 and UDF_7. Thus, the proposed method gives 100% fault coverage, which cannot see in the any other existing method.

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